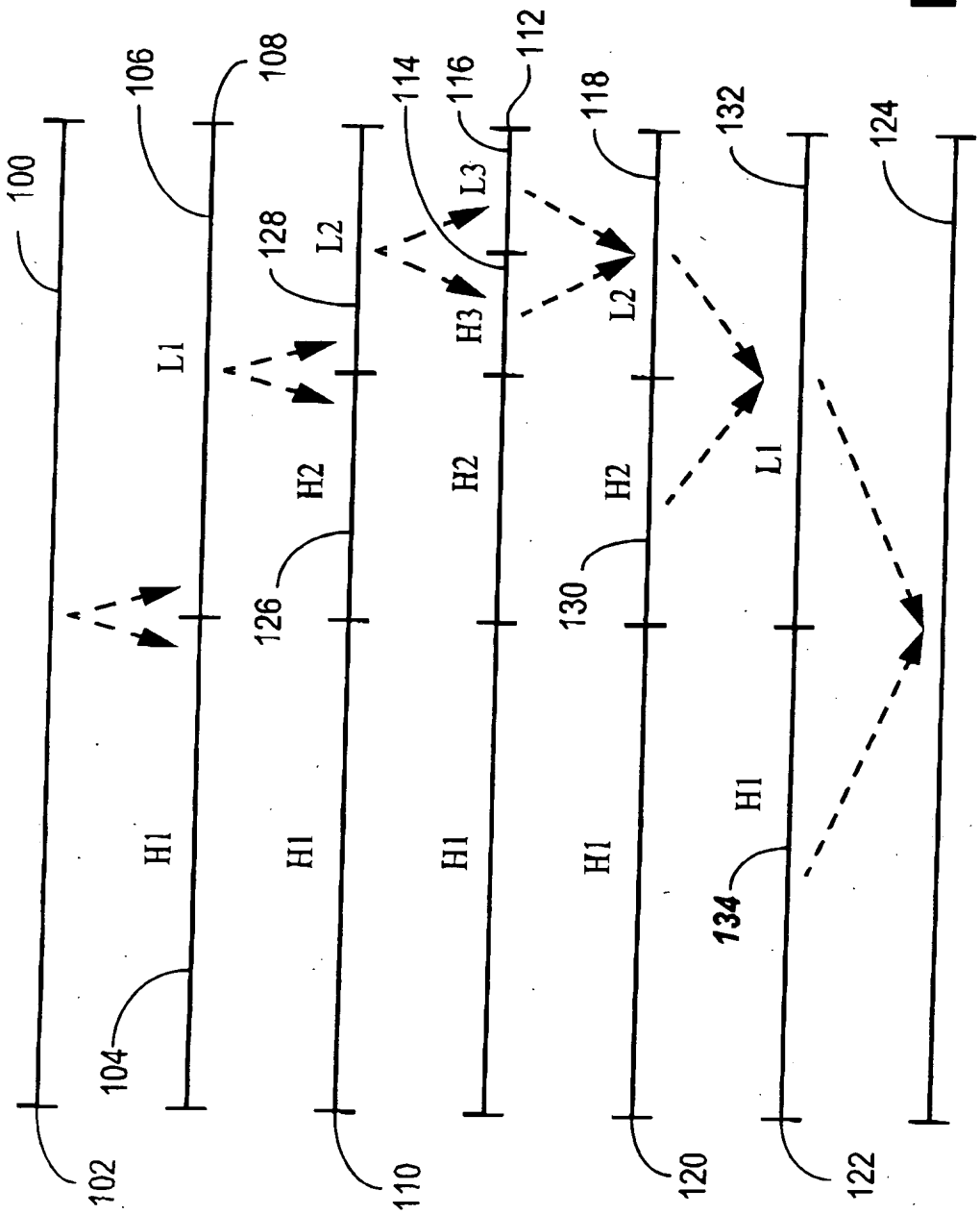

100
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
132
134
H1
H2
H3
L1
L2
L3

Fig. 1

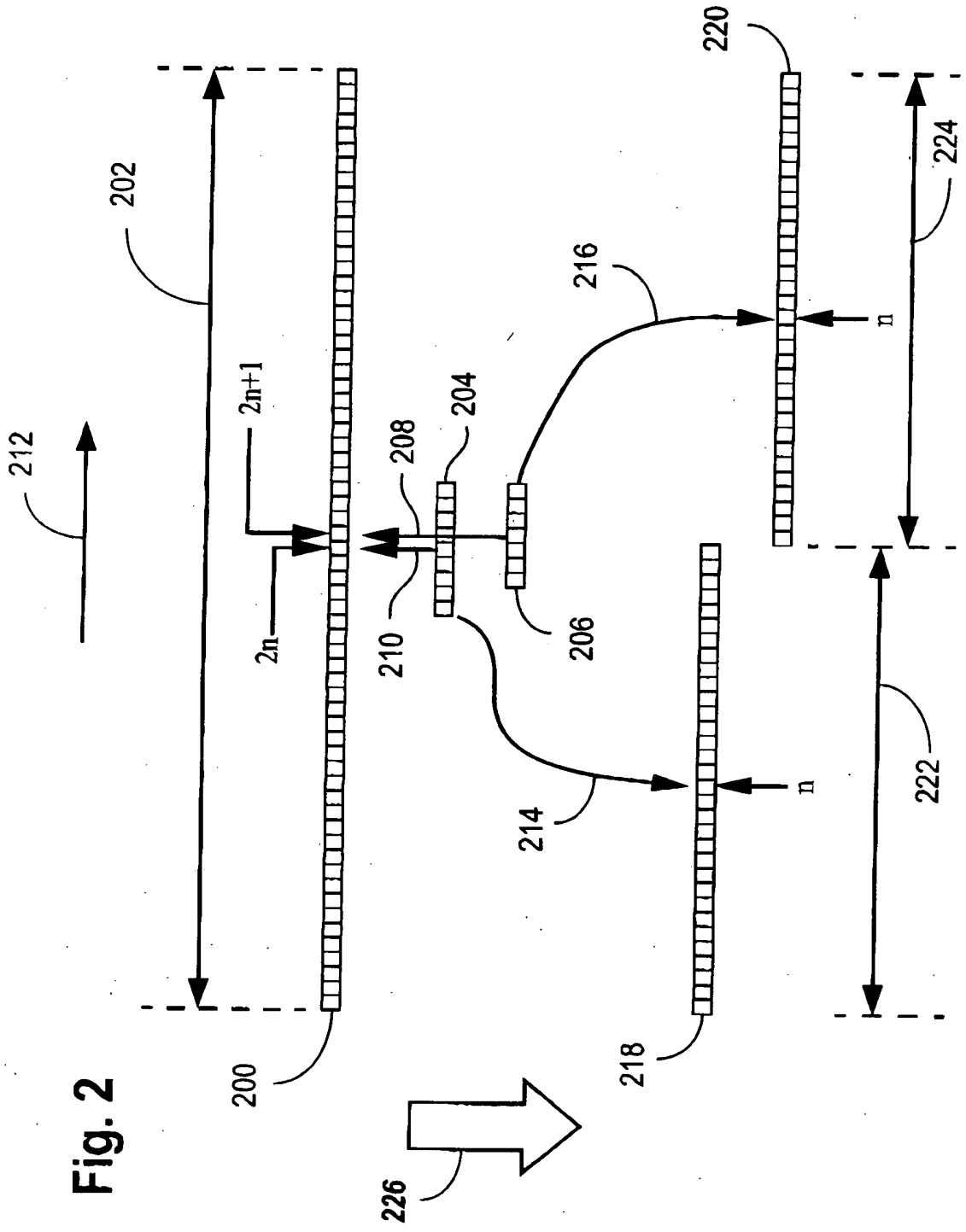


Fig. 2

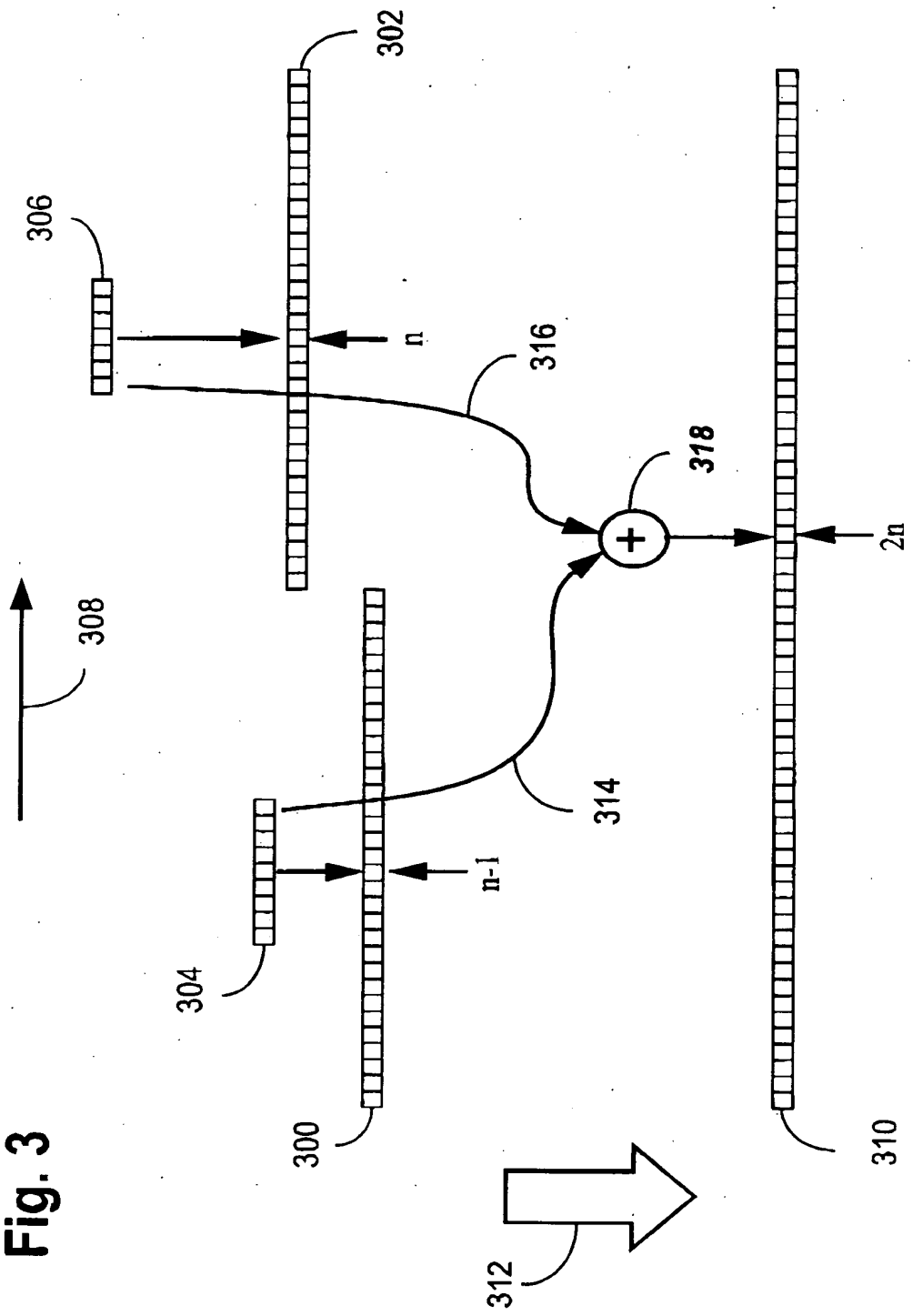


Fig. 3

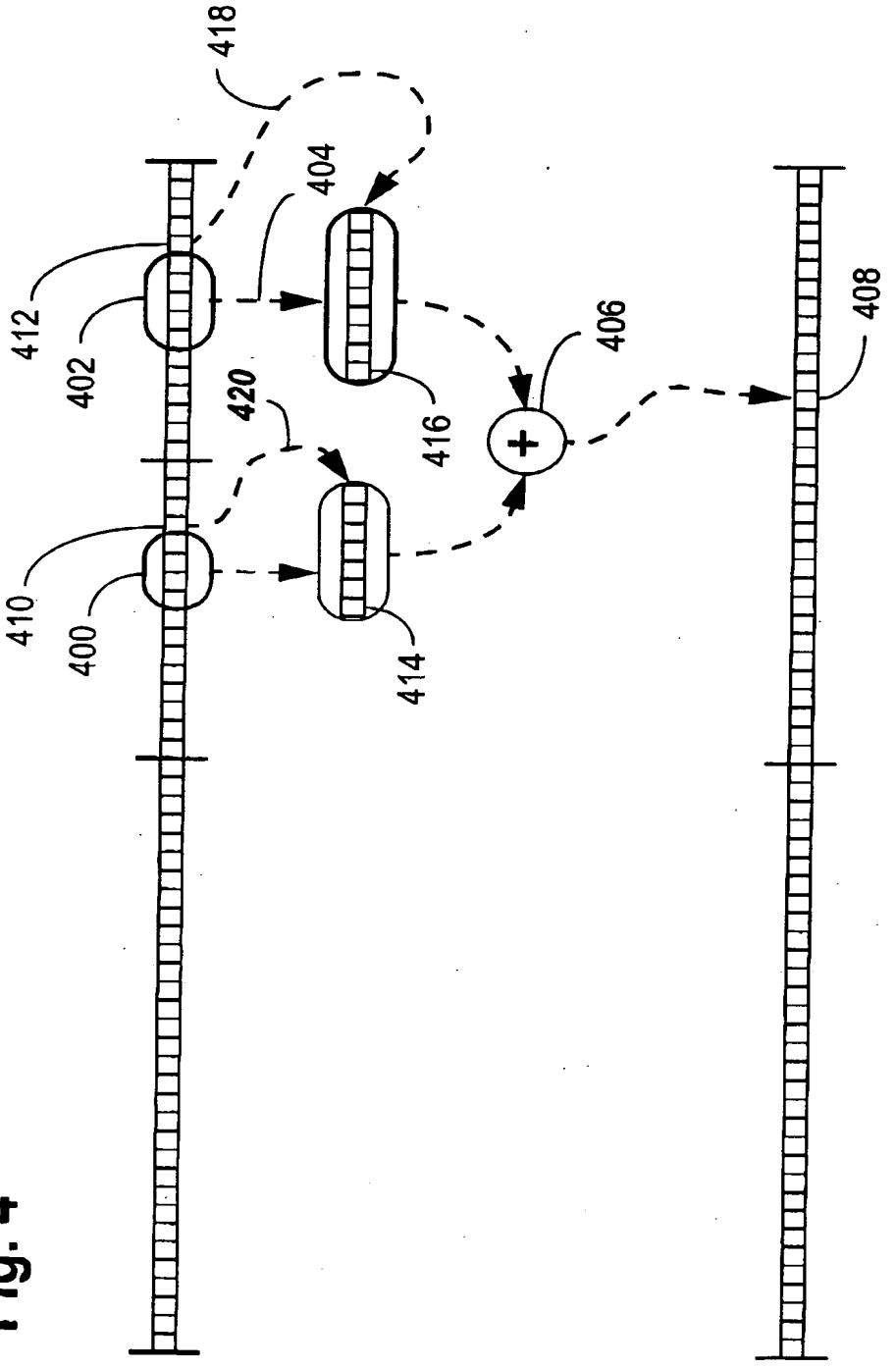


Fig. 4

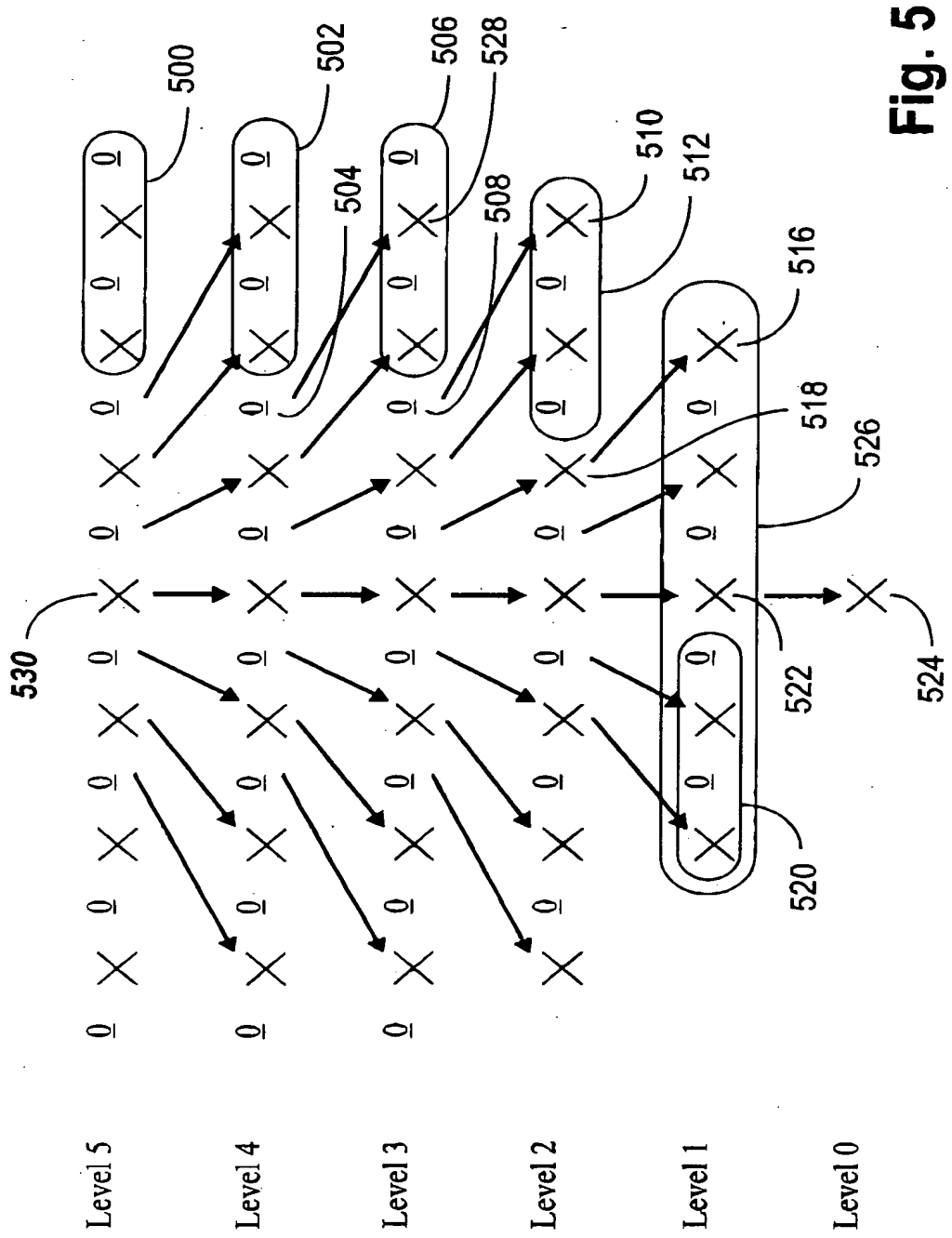

Level 5
Level 4
Level 3
Level 2
Level 1
Level 0
500
502
504
506
508
510
512
516
518
520
522
524
526
528
530

Fig. 5

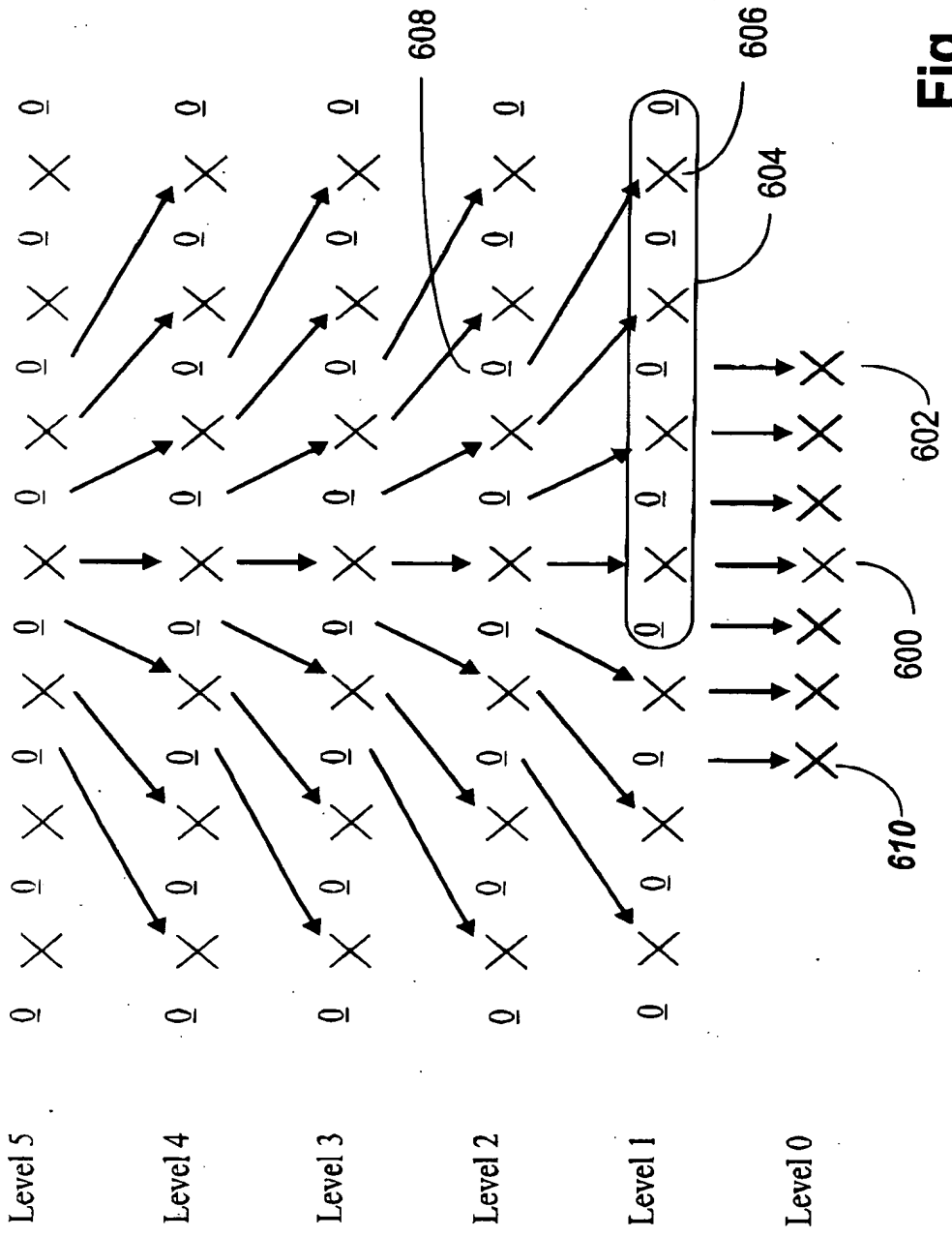

Level 5
Level 4
Level 3
Level 2
Level 1
Level 0
608
606
604
602
600
610

Fig. 6

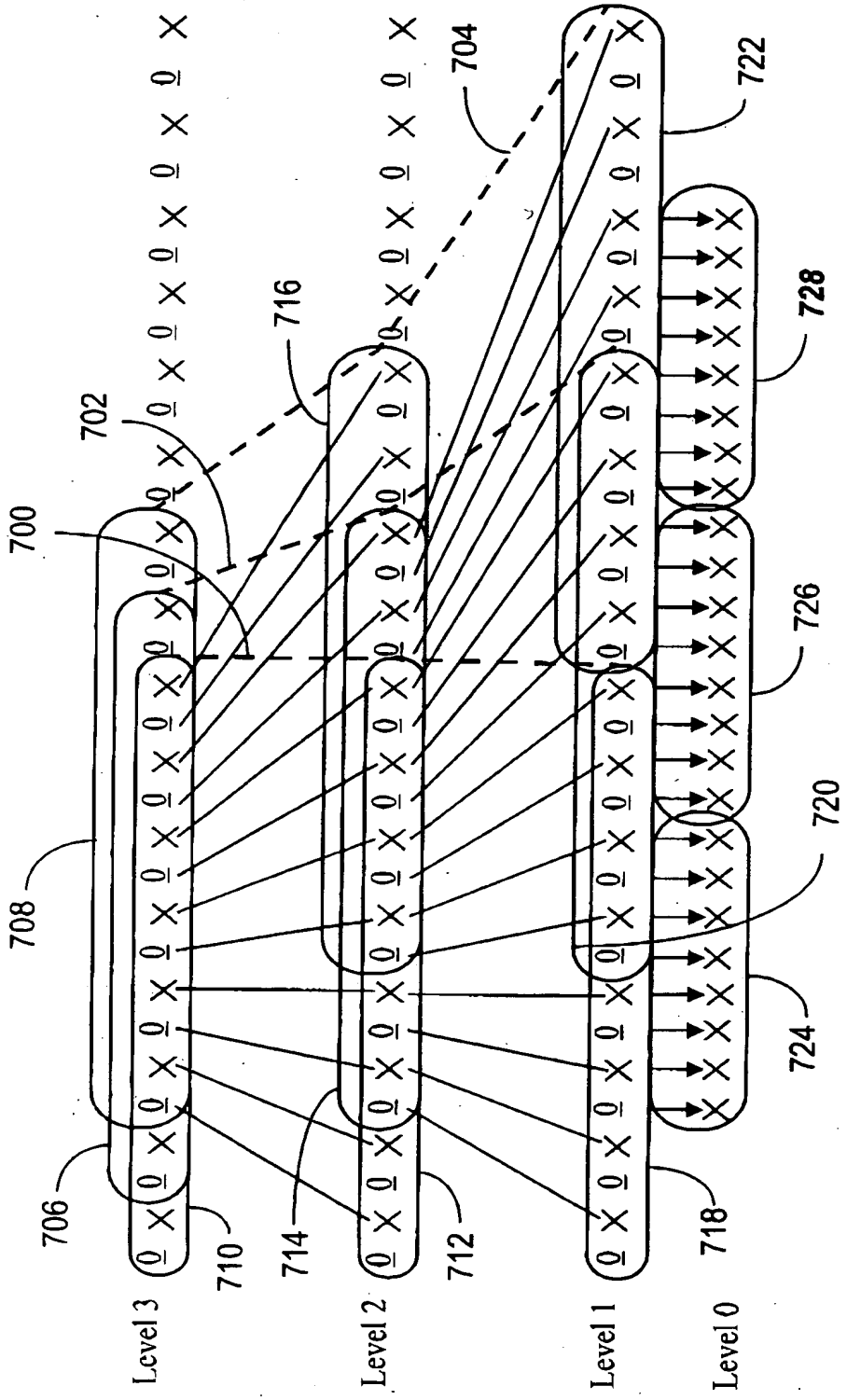

700
702
704
706
708
710
712
714
716
718
720
722
724
726
728
Level 3
Level 2
Level 1
Level 0

Fig. 7

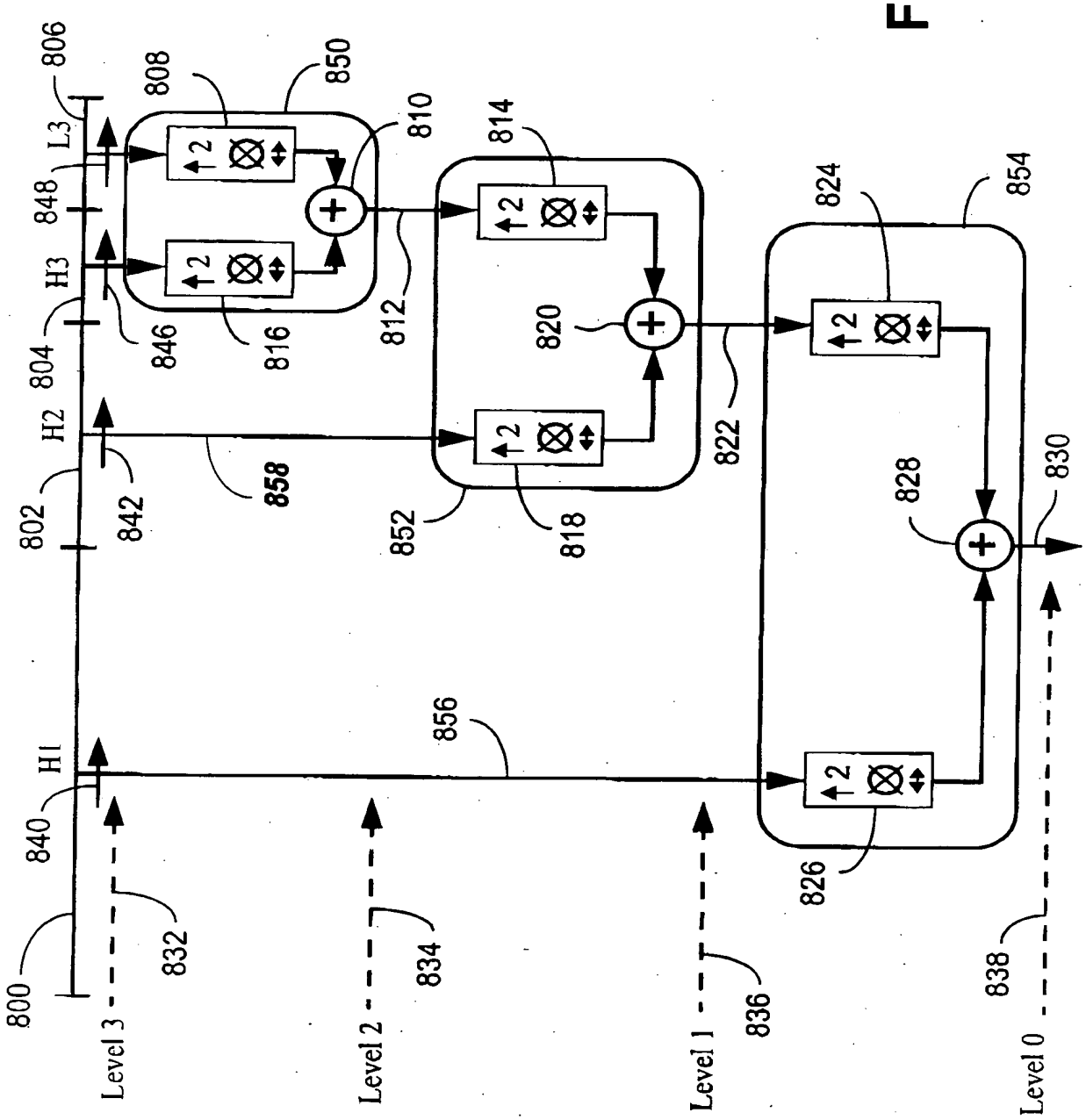

806
808
850
L3
848
H3
804
846
816
812
810
814
820
824
854
H2
802
842
858
852
818
822
828
830
H1
840
856
826
800
832
834
836
838
Level 3
Level 2
Level 1
Level 0

Fig. 8

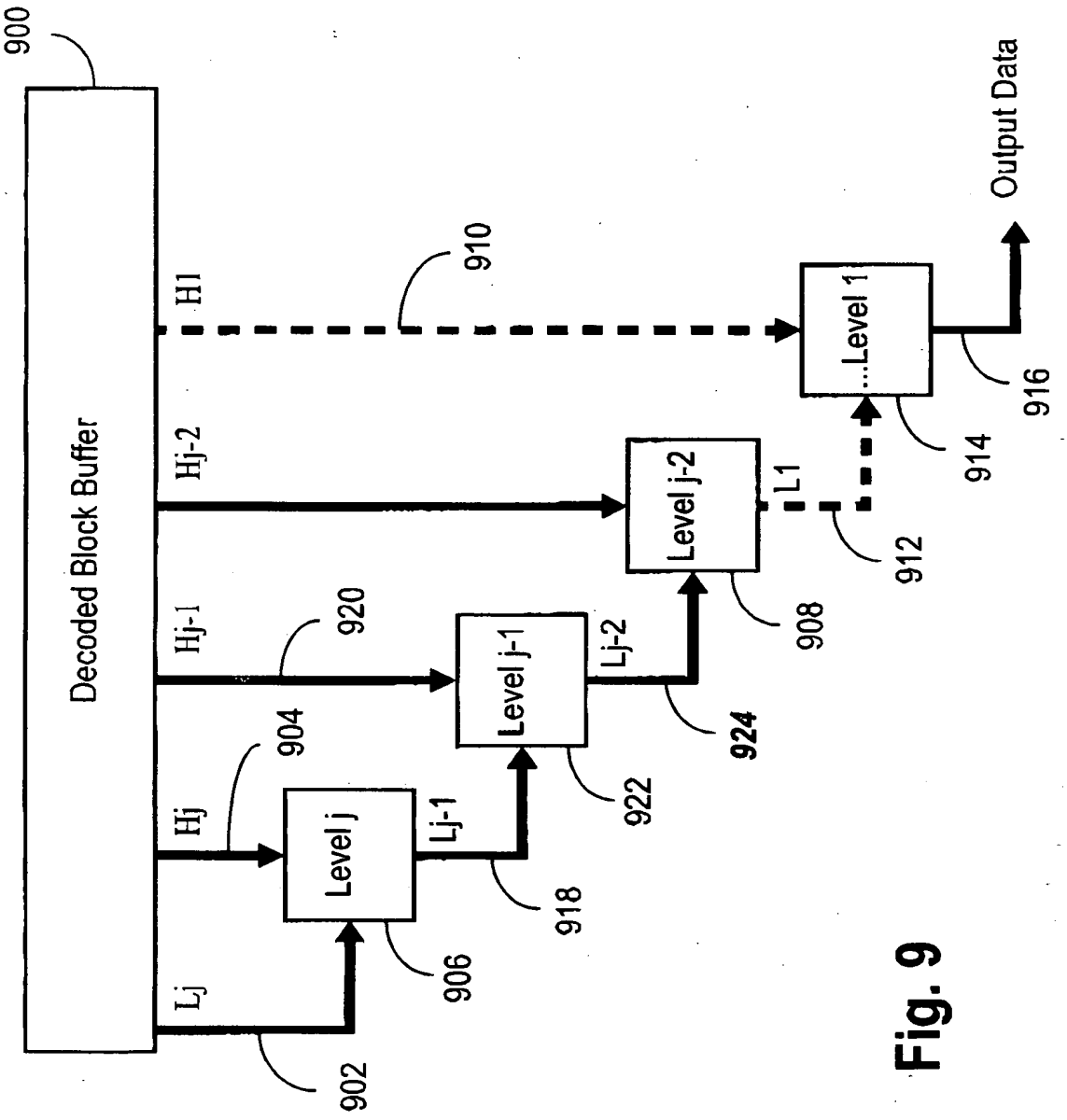

900
Decoded Block Buffer
H1
910
Hj-2
Hj-1
920
Hj
904
Lj
902
Level j
906
Lj-1
918
Level j-1
922
Lj-2
924
Level j-2
908
L1
912
...Level 1
914
916
Output Data

Fig. 9

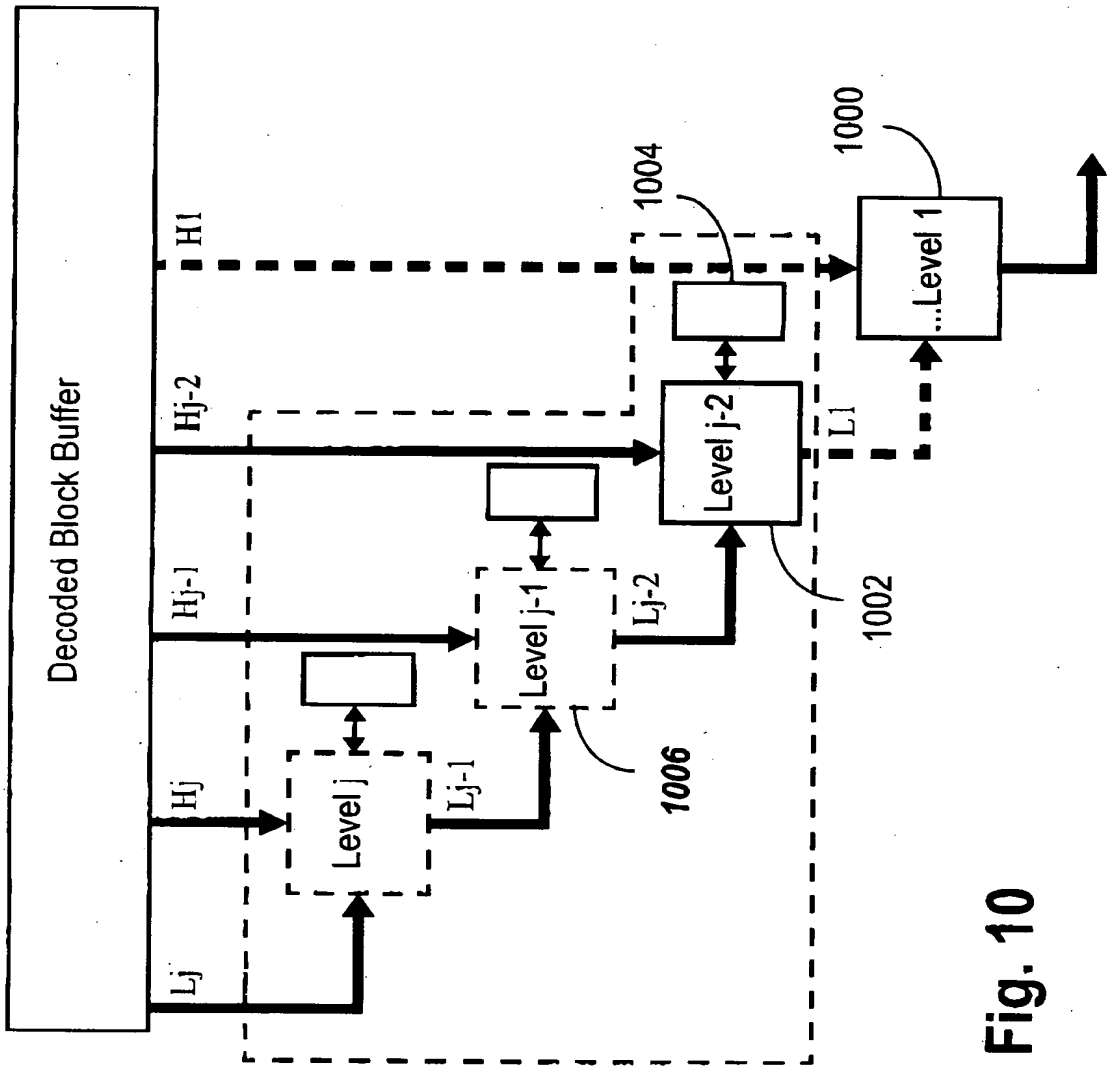

Decoded Block Buffer
H1
Hj-2
Hj-1
Hj
Lj
Level j
Lj-1
Level j-1
Lj-2
Level j-2
L1
...Level 1
1000
1004
1002
1006

Fig. 10

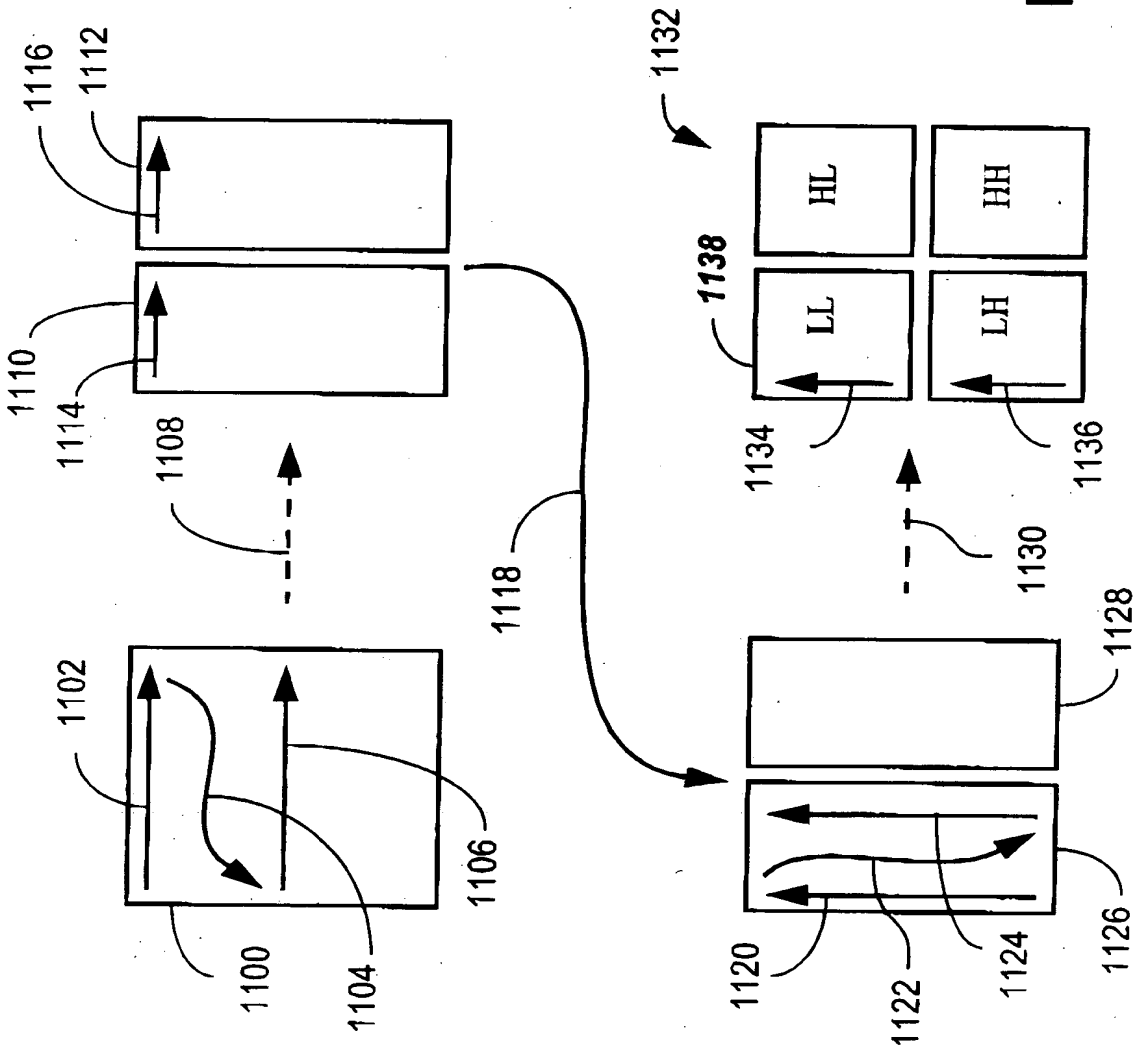

1116
1112
1110
1114
1108
1102
1100
1104
1106
1118
1132
1138
HL
HH
LL
LH
1134
1136
1130
1128
1120
1122
1124
1126

Fig. 11

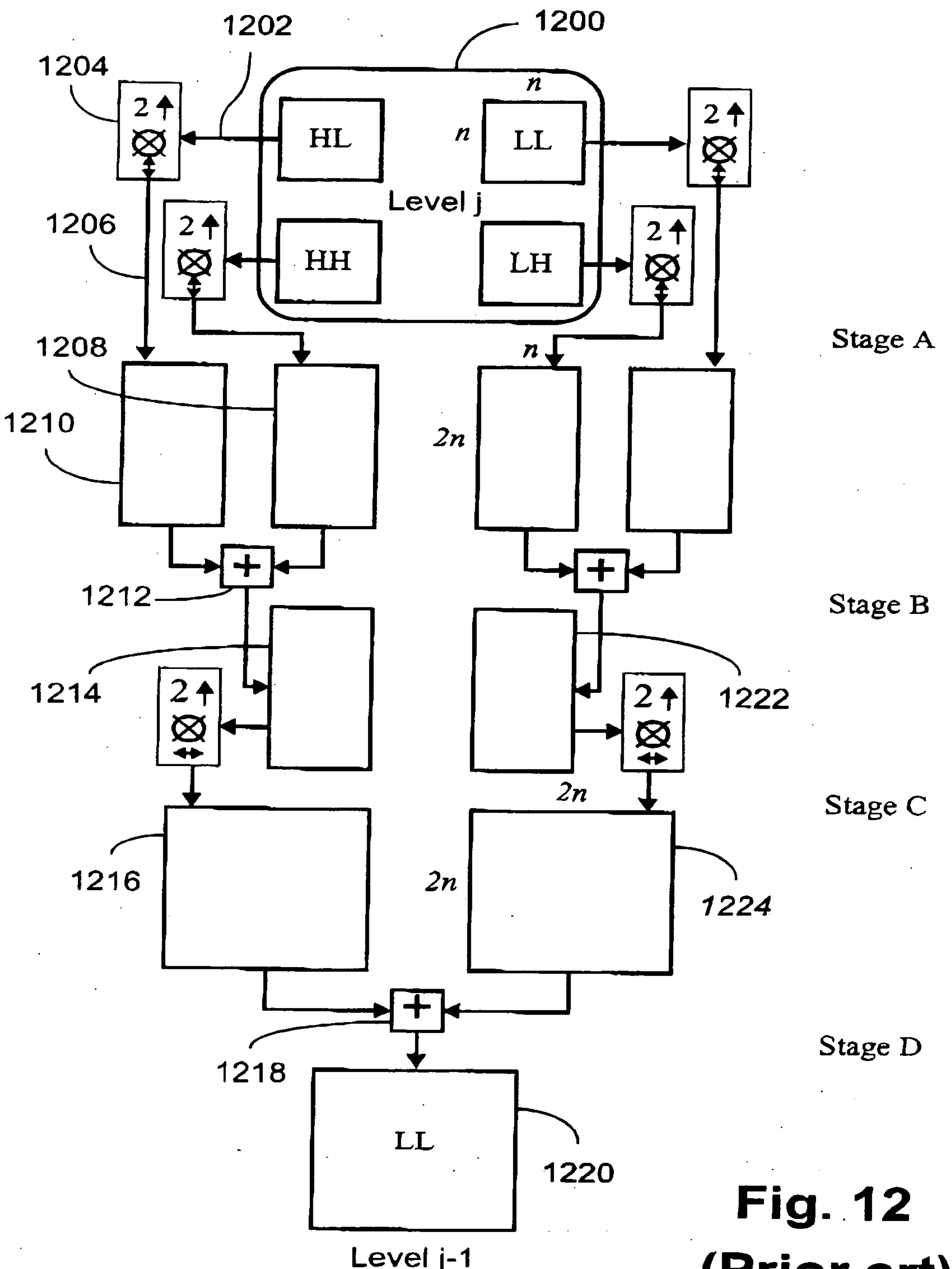


Fig. 12
(Prior art)

09730508 .120700

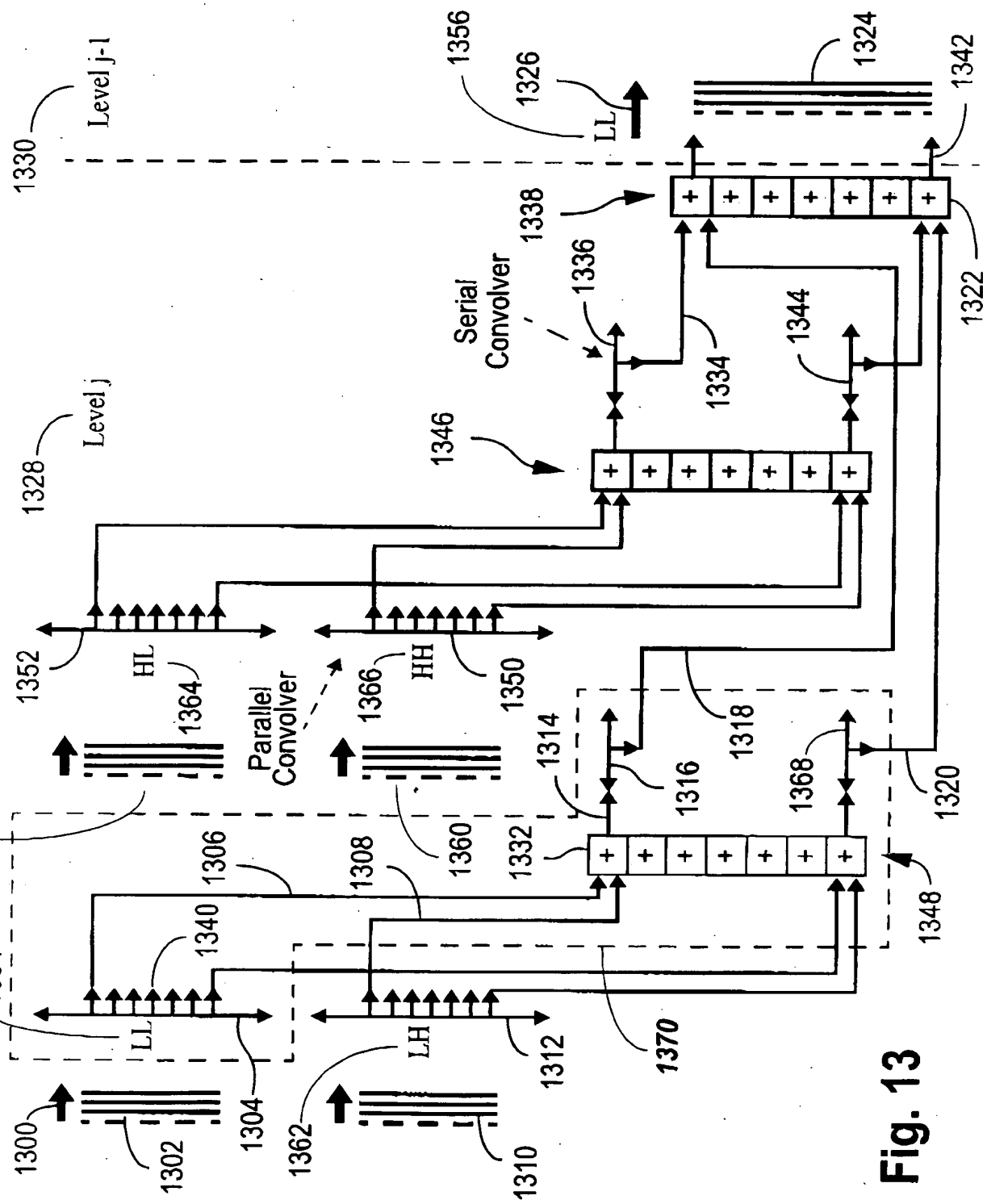

Level j-1
Level j
Serial Convolver
Parallel Convolver
LL
LH
HL
HH
1300
1302
1304
1306
1308
1310
1312
1314
1316
1318
1320
1322
1324
1326
1328
1330
1332
1334
1336
1338
1340
1342
1344
1346
1348
1350
1352
1354
1356
1358
1360
1362
1364
1366
1368
1370

Fig. 13

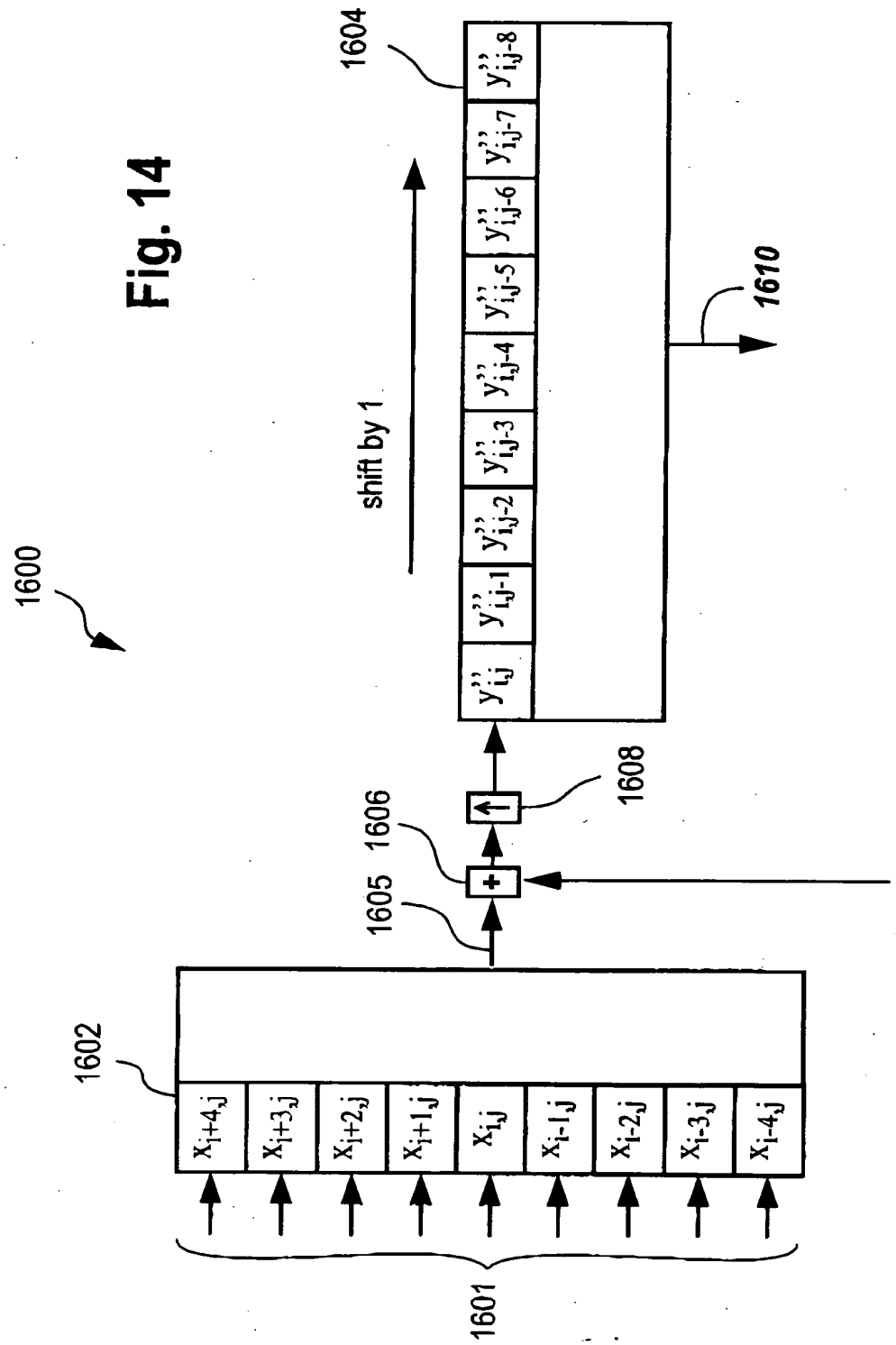

1600
1601
1602
1604
1605
1606
1608
1610
shift by 1
$x_{i+4,j}$ $x_{i+3,j}$ $x_{i+2,j}$ $x_{i+1,j}$ $x_{i,j}$ $x_{i-1,j}$ $x_{i-2,j}$ $x_{i-3,j}$ $x_{i-4,j}$
$y''_{i,j}$ $y''_{i,j-1}$ $y''_{i,j-2}$ $y''_{i,j-3}$ $y''_{i,j-4}$ $y''_{i,j-5}$ $y''_{i,j-6}$ $y''_{i,j-7}$ $y''_{i,j-8}$

Fig. 14

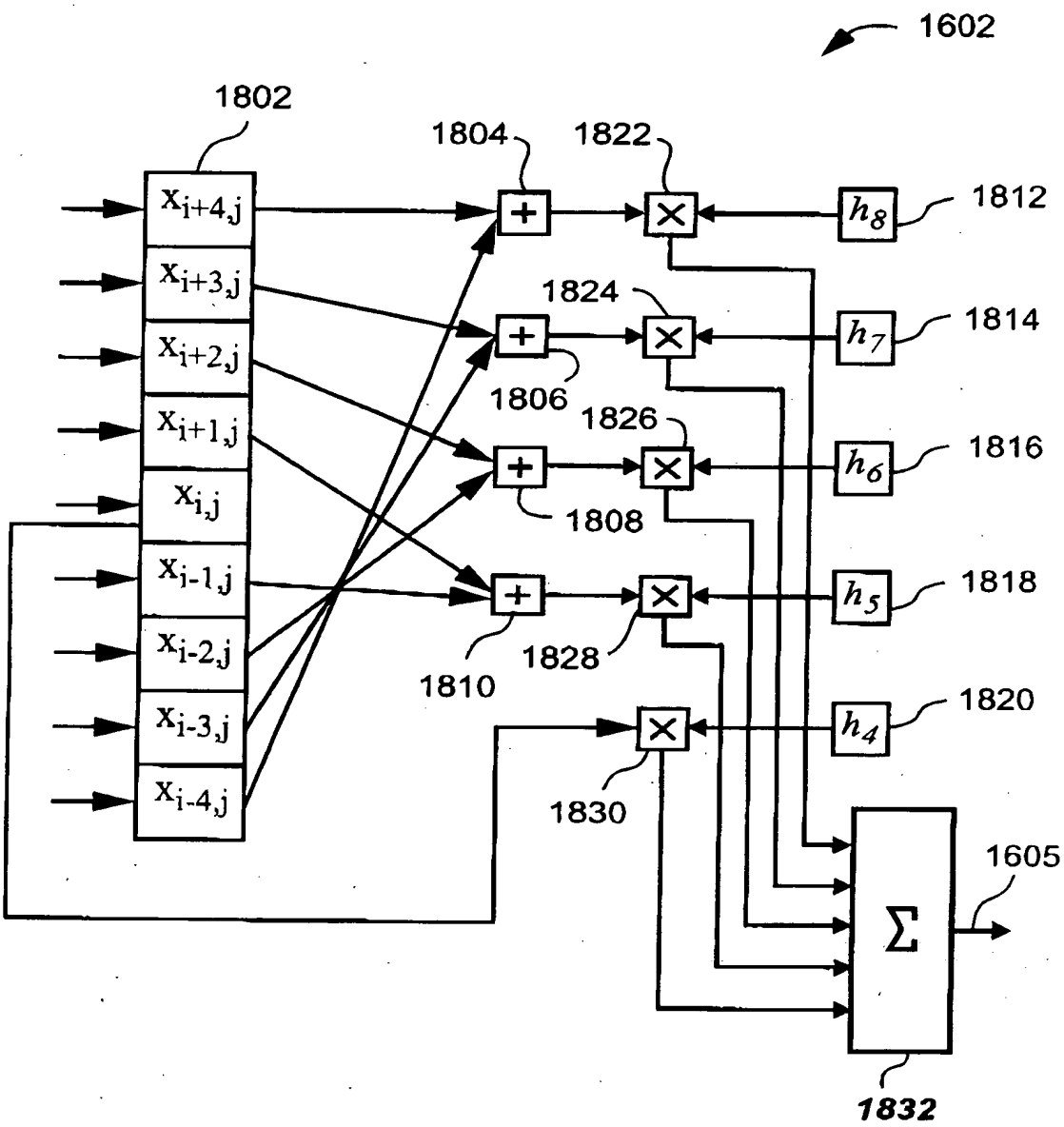

1602
1802
1804
1822
1812
1824
1814
1806
1826
1816
1808
1818
1810
1828
1820
1830
1605
1832
$x_{i+4,j}$
$x_{i+3,j}$
$x_{i+2,j}$
$x_{i+1,j}$
$x_{i,j}$
$x_{i-1,j}$
$x_{i-2,j}$
$x_{i-3,j}$
$x_{i-4,j}$
h_8
h_7
h_6
h_5
h_4
Σ

Fig. 15

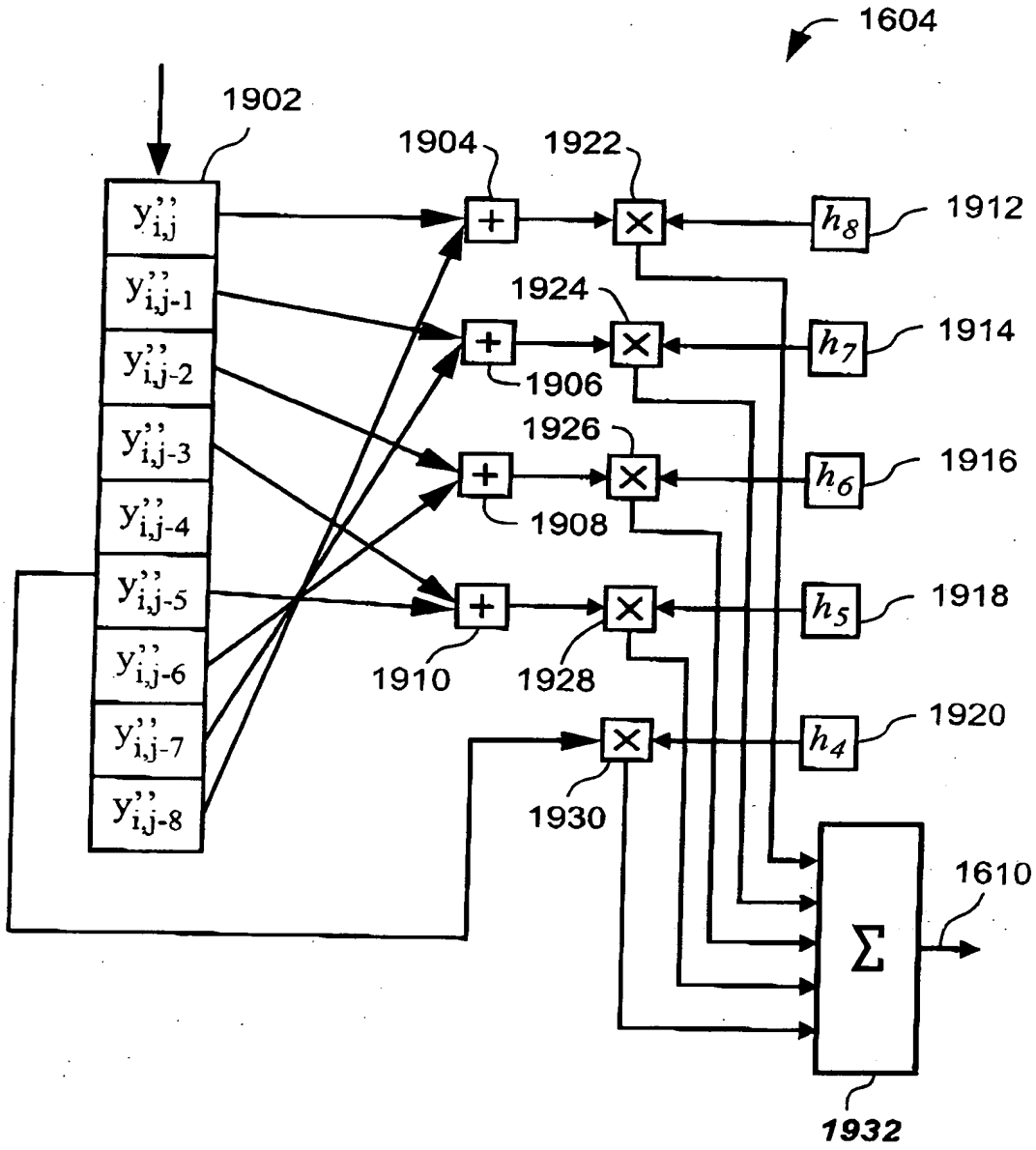

1604
1902
1904
1922
1912
1924
1914
1906
1926
1916
1908
1918
1910
1928
1920
1930
1610
1932
$y''_{i,j}$
$y''_{i,j-1}$
$y''_{i,j-2}$
$y''_{i,j-3}$
$y''_{i,j-4}$
$y''_{i,j-5}$
$y''_{i,j-6}$
$y''_{i,j-7}$
$y''_{i,j-8}$
h_8
h_7
h_6
h_5
h_4
Σ

Fig. 16

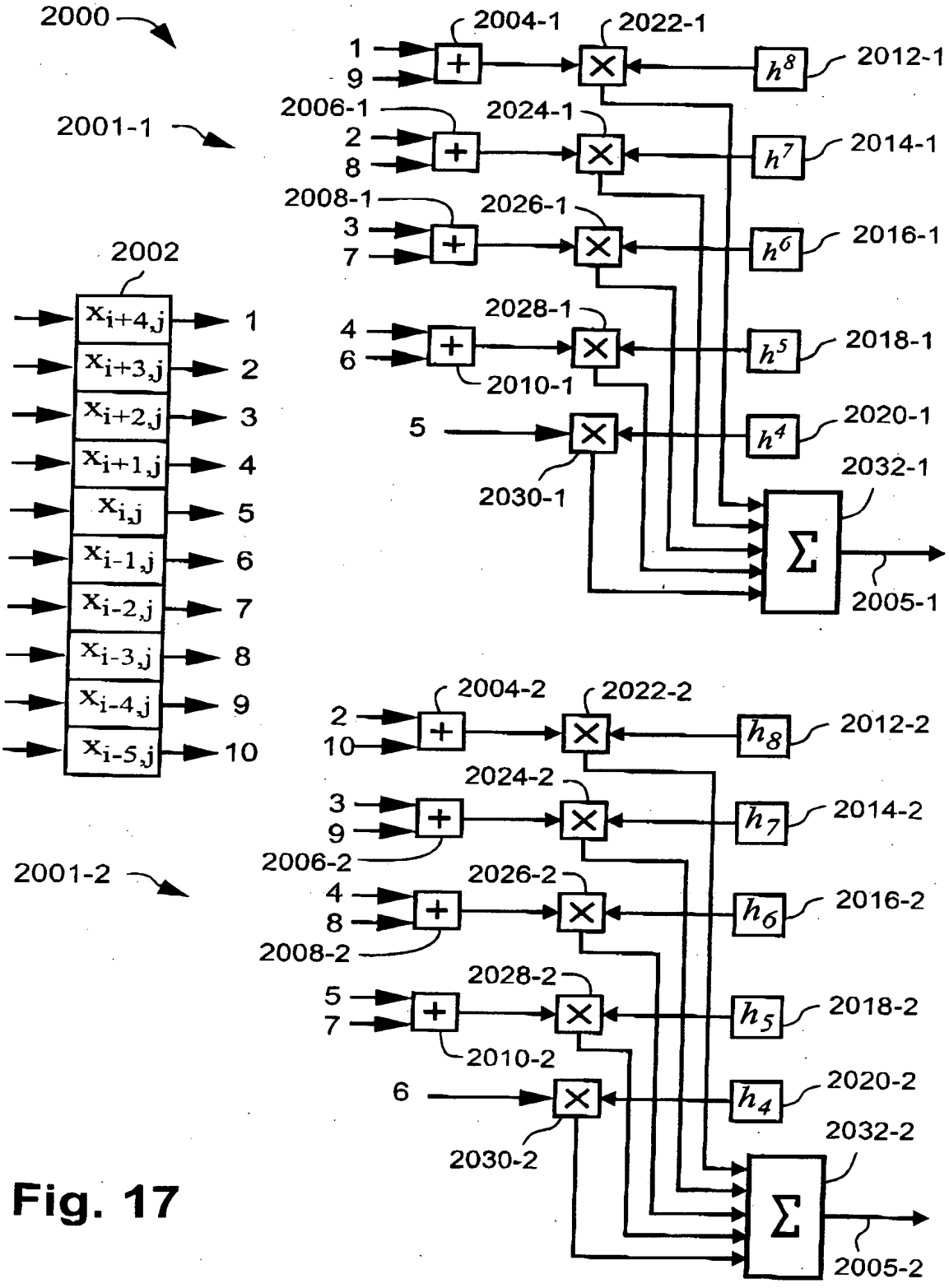

2000
2001-1
2001-2
2002
2004-1
2022-1
2006-1
2024-1
2008-1
2026-1
2028-1
2010-1
2030-1
2032-1
2005-1
2012-1
2014-1
2016-1
2018-1
2020-1
2004-2
2022-2
2006-2
2024-2
2008-2
2026-2
2028-2
2010-2
2030-2
2032-2
2005-2
h^8
h^7
h^6
h^5
h^4
h_8
h_7
h_6
h_5
h_4
$x_{i+4,j}$
$x_{i+3,j}$
$x_{i+2,j}$
$x_{i+1,j}$
$x_{i,j}$
$x_{i-1,j}$
$x_{i-2,j}$
$x_{i-3,j}$
$x_{i-4,j}$
$x_{i-5,j}$
Σ

Fig. 17

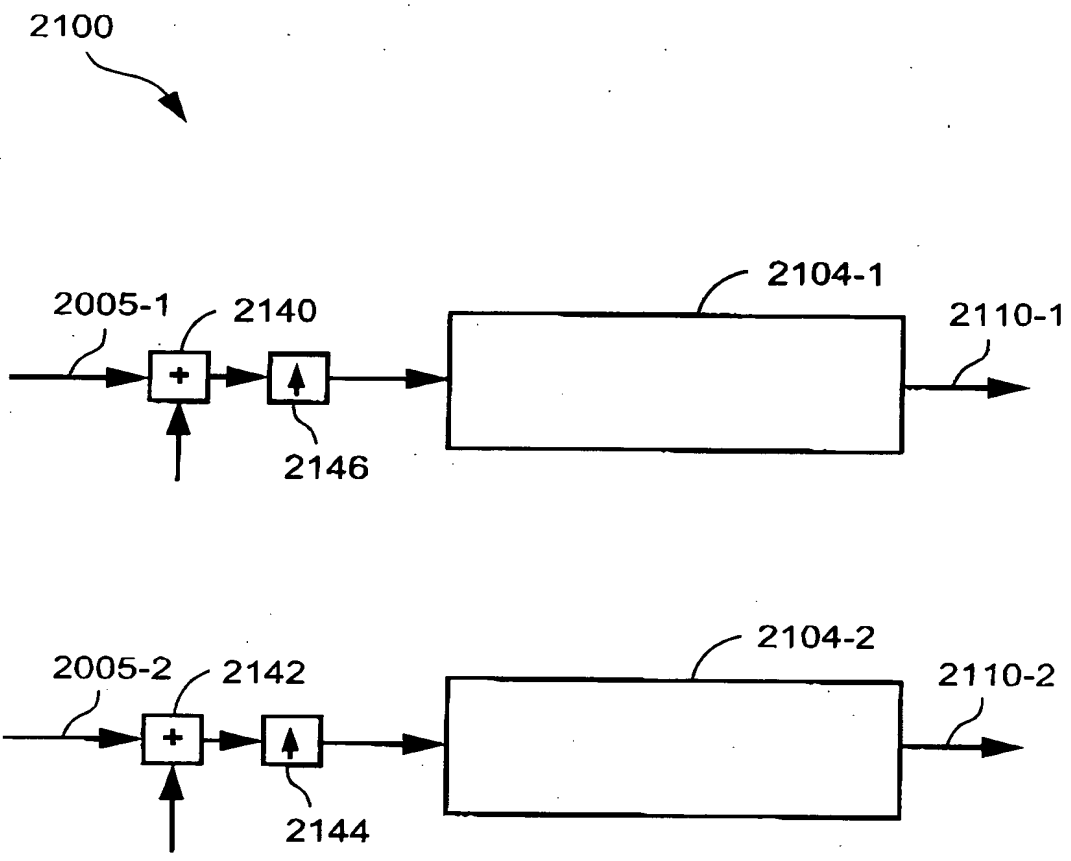
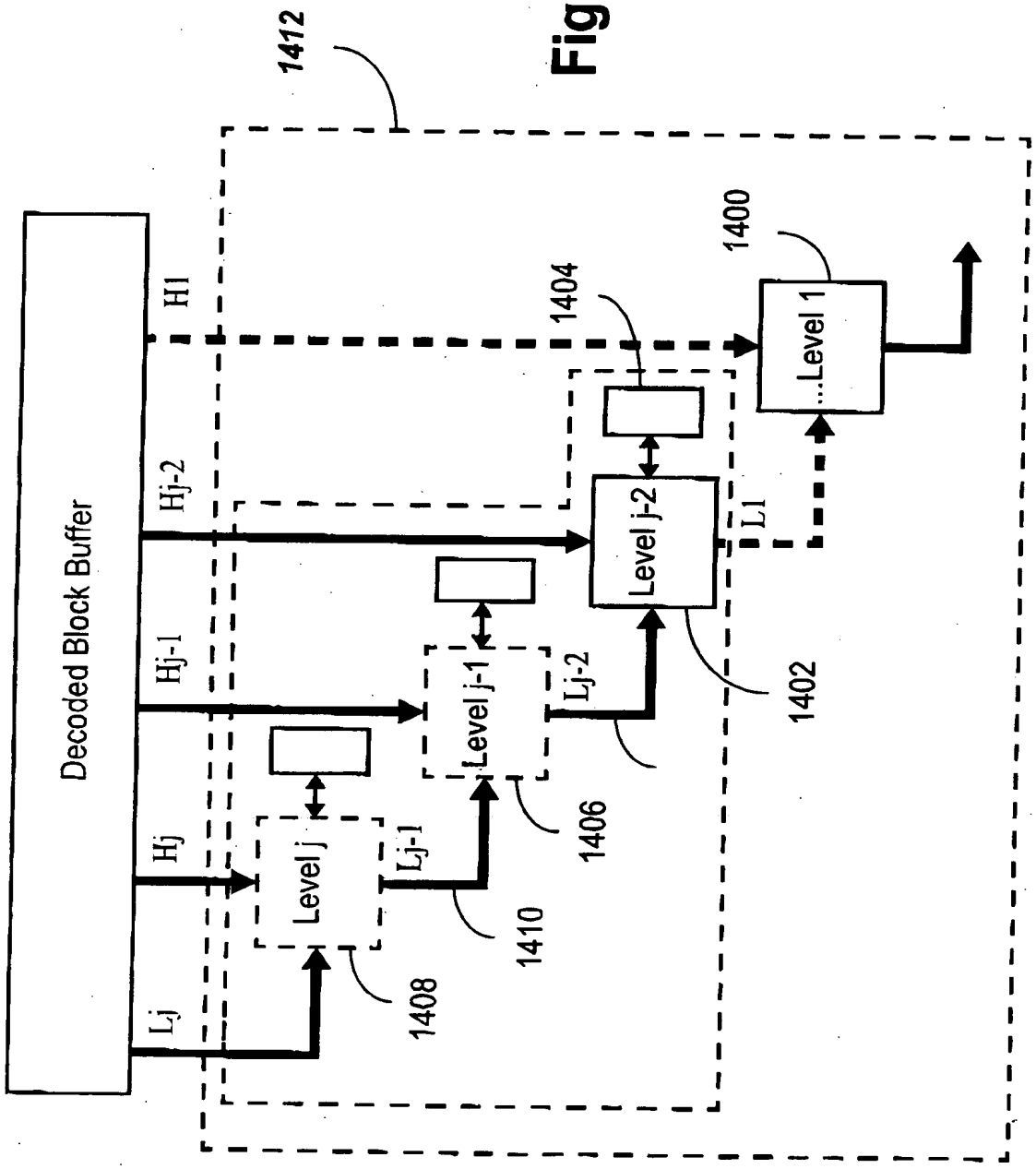

2100
2005-1
2140
2104-1
2110-1
2146
2005-2
2142
2104-2
2110-2
2144

Fig. 18

Fig. 19


1412
Decoded Block Buffer
H1
Hj-2
Hj-1
Hj
Lj
1400
Level 1
1404
Level j-2
L1
1402
Level j-1
Lj-2
1406
Level j
Lj-1
1410
1408

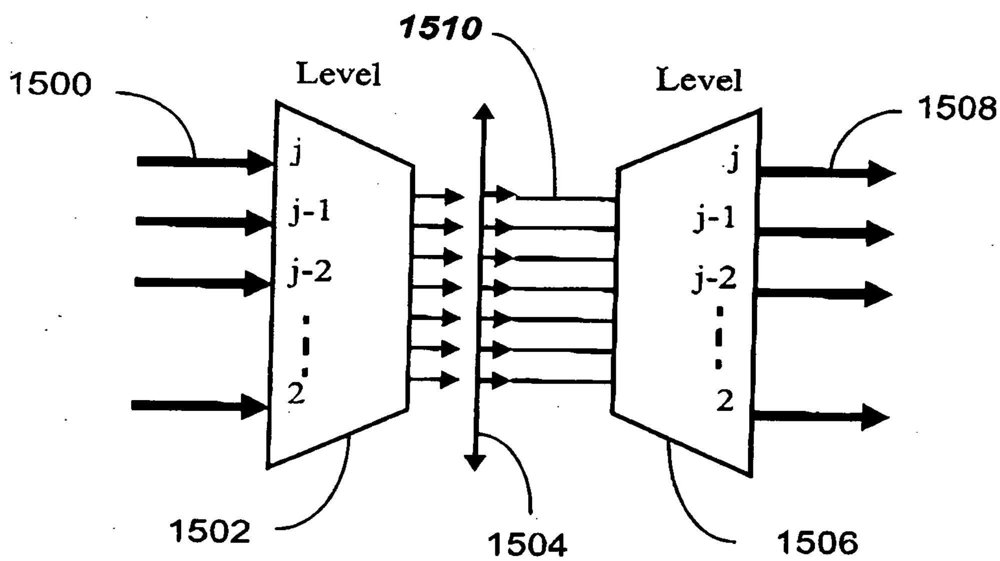
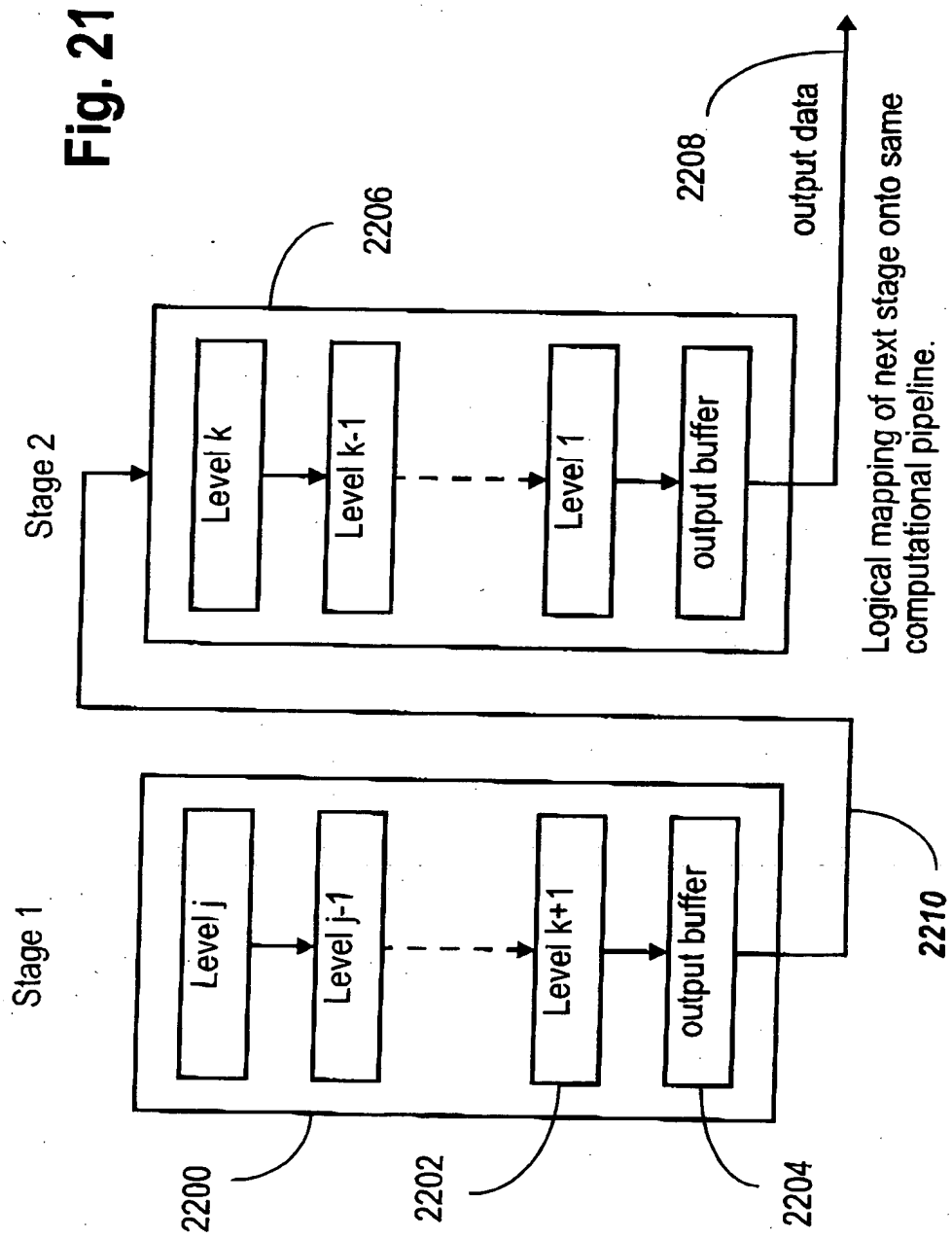


Fig. 20

09730558 .120700

Fig. 21


Stage 1
Level j
Level j-1
Level k+1
output buffer
2200
2202
2204
2210
Stage 2
Level k
Level k-1
Level 1
output buffer
2206
2208
output data
Logical mapping of next stage onto same computational pipeline.

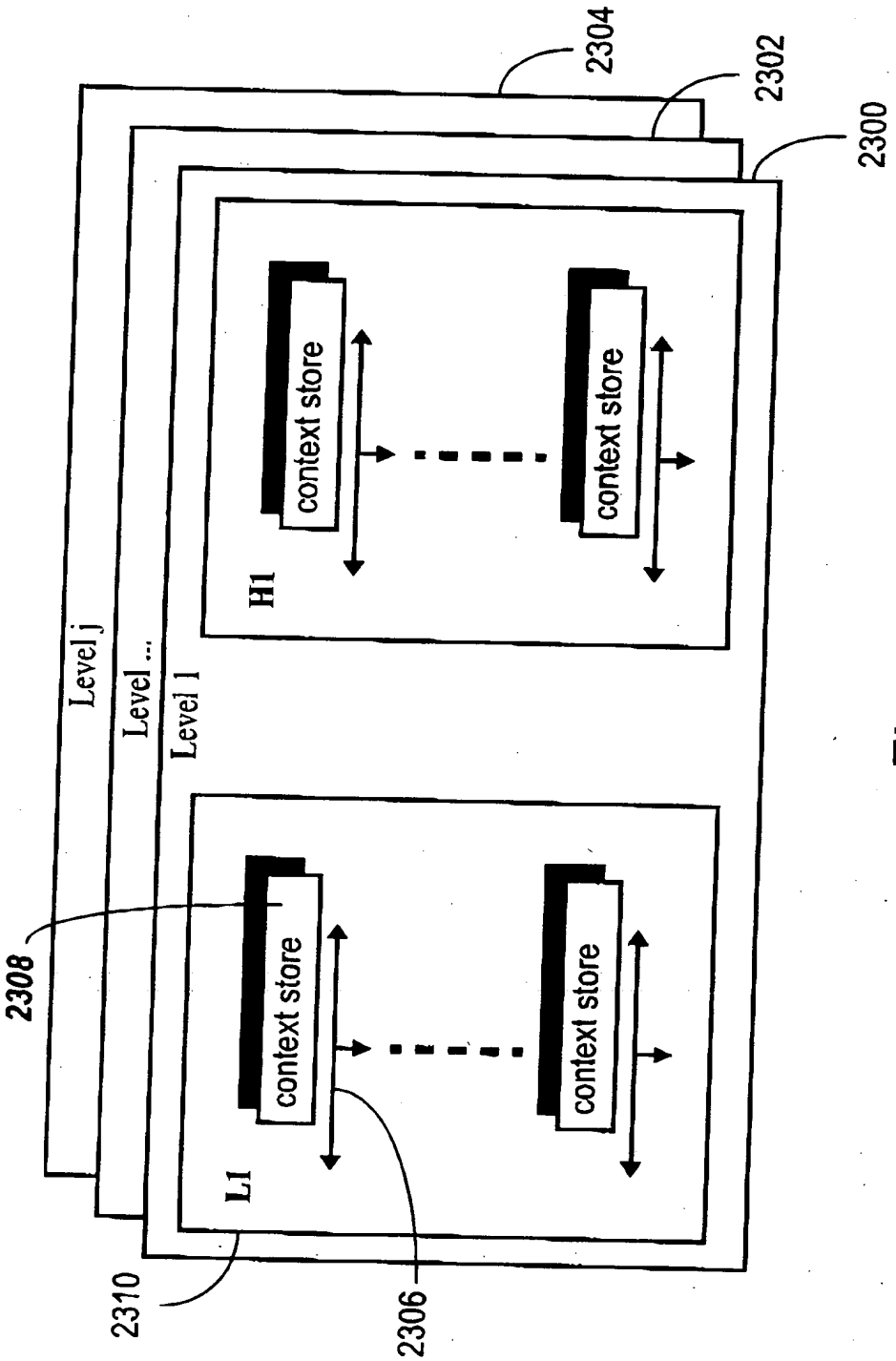

2304
2302
2300
Level j
Level ...
Level 1
H1
context store
context store
2308
L1
context store
context store
2310
2306

Fig. 22

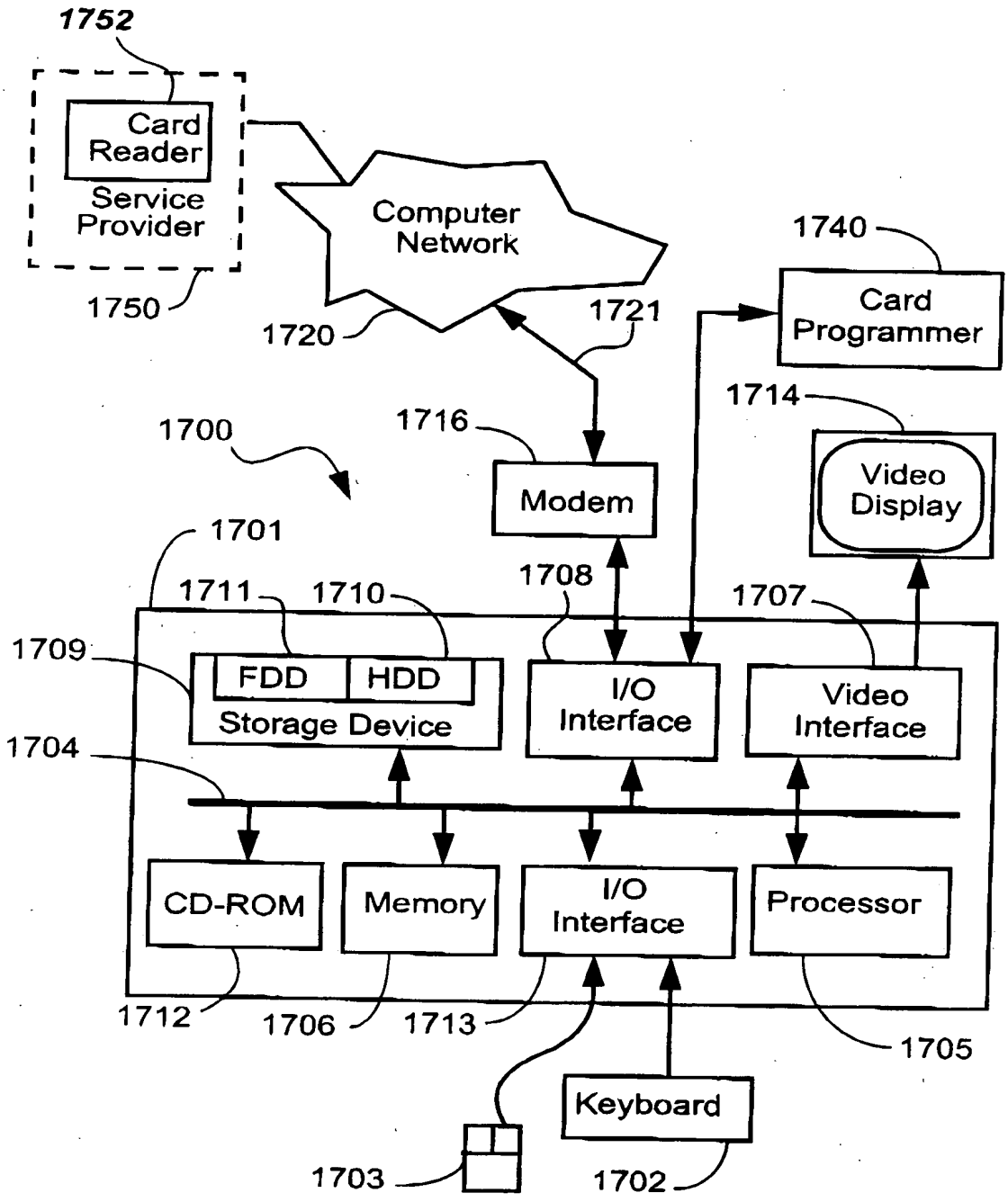

1752
Card Reader
Service Provider
1750
Computer Network
1720
1721
1740
Card Programmer
1714
Video Display
1700
1716
Modem
1701
1708
1711
1710
1707
1709
FDD
HDD
Storage Device
I/O Interface
Video Interface
1704
CD-ROM
Memory
I/O Interface
Processor
1712
1706
1713
1705
Keyboard
1703
1702

Fig. 23